AMENDMENTS TO THE CLAIMS

1. (currently amended) An integrated circuit device comprising:

an array of ~~erasable~~ flash memory cells, said cells comprising a source, a drain and a stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer, wherein a region under said stacked gate structure comprises overlapping lateral diffusions of implantation regions of said source and said drain;

a common source line coupled with said source; and

a source contact disposed outside of said common source line and coupled with said source, wherein said source contact is coupled to said common source line under said stacked gate structure through a particular drain, and wherein said source contact is disposed in a row with drain contacts.

2. (original) The integrated circuit device of Claim 1 comprising substantially straight word lines.

3. (original) The integrated circuit device of Claim 1 wherein said common source line has a substantially uniform width within said array of cells.

4-5. (canceled)

6. (original) The integrated circuit device of Claim 1 wherein said integrated circuit device comprises a non-volatile memory.

7. (previously presented) The integrated circuit device of Claim 6 wherein said charge trapping layer is a floating gate.

8. (currently amended) An integrated circuit device comprising ~~an erasable~~a first non-volatile flash memory cell comprising:

a first stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer;

dopants disposed on either sides of said first stacked gate structure; and

a first region under said first stacked gate structure comprising overlapping lateral diffusions of source and drain implantation regions, ~~wherein dopants are~~

~~implanted on either sides of said first stacked gate structure,~~ wherein said source and drain implantation regions are able to conduct independent of any voltage applied to said first stacked gate structure, wherein said source implantation region is coupled to a common source line, wherein a first source contact is disposed outside of said common source line and coupled with said source implantation region, wherein said first source contact is coupled to said common source line under said first stacked gate structure through said drain implantation region, and wherein said first source contact is disposed in a row of drain contacts.

9.-10. (cancelled)

11. (previously presented) The integrated circuit device of Claim 8 further comprising a second non-volatile flash memory cell comprising a second stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer, wherein a second region under said second stacked gate structure comprises overlapping lateral diffusions of source and drain implantation regions.

12. (previously presented) The integrated circuit device of Claim 11 wherein the source region associated with said second stacked gate structure is coupled to a second source contact, wherein said second source contact is coupled with said common source line and disposed outside of said common source line, wherein said second source contact is coupled to said common source line under said second stacked gate structure, and wherein said second source contact is disposed in a row of drain contacts.

13-20. (cancelled)